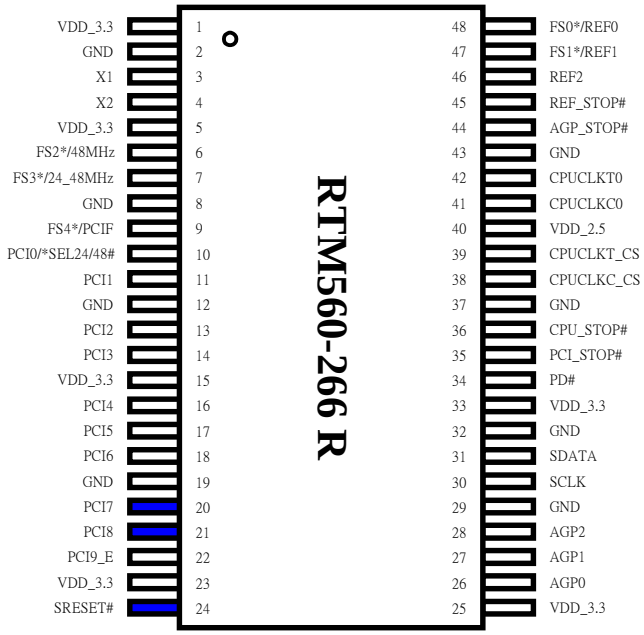
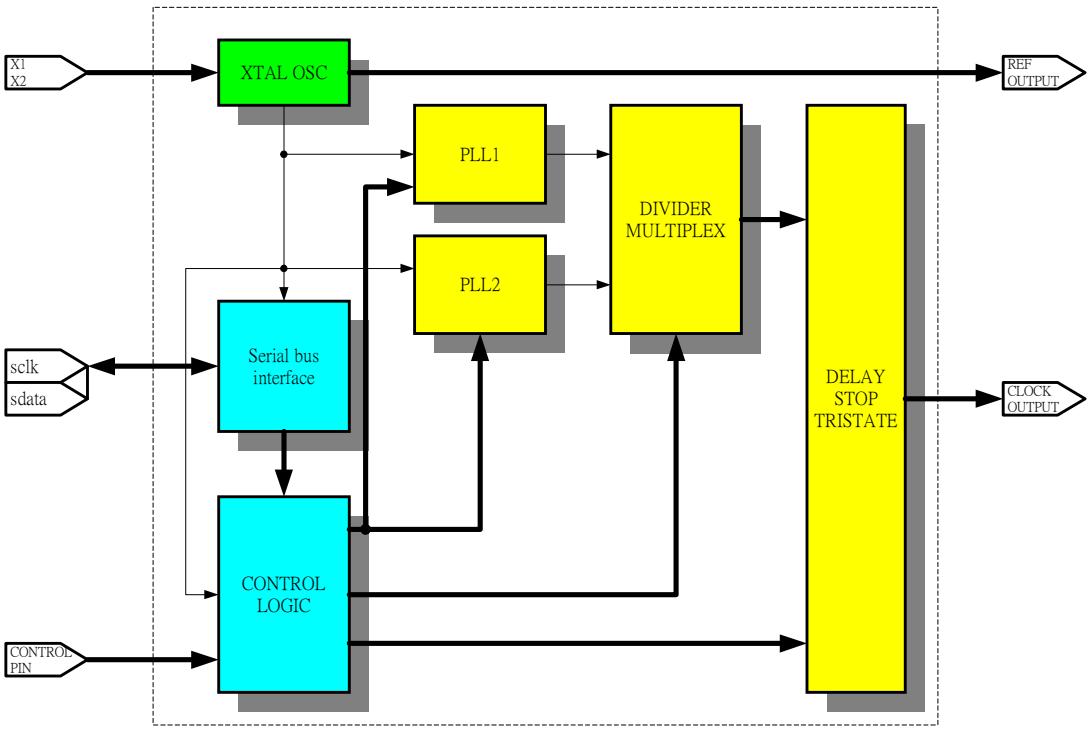
General Description

The RTM 560-266R is a single chip frequency generator for VIA KT266 system. The clock chip provides standard serial bus for programming device function. Based on the function above, the spread spectrum can be enable for reducing EMI. And RTM 560-266R also builds in the testability function.

Features

- Support Up to 200 MHz frequency.
- Power Down feature.
- Spread Spectrum for EMI control.
- Output features:
  - 1 pairs – CPU differential open drain.
  - 1 pairs - CPU differential@2.5V.
  - 11- PCI @3.3V.
  - 1- 48MHz, @3.3V fixed.
  - 1- 24_48# MHz, @3.3V fixed.
  - 3- REF @3.3V, 14.318MHz.
  - 3- AGP @3.3V





RTM DDR solution :

RTM560-250R+RTM580-251R(4DDR/2SDR) (2DDR+2SDR) SSOP-48

RTM560-250R+RTM580-256R(4DDR/2SDR) (3DDR+2SDR) SSOP-56

RTM560-250R+RTM580-255R(4DDR/3SDR) (2DDR+3SDR) SSOP-48

RTM560-250R+RTM580-228R(2DDR/3SDR) SSOP-28

Pin Description

Pin Name	PIN	Type	Description
REF_0/FS0*	48	I/O	***Reference Clock0 /Frequency Selection 0:*** 3.3V 14.318 MHz clock output. This pin also serves as the select strap to determine device's operating frequency as described in frequency Table. Pull high 120k.
REF_1/FS1*	47	I/O	***Reference Clock1 /Frequency Selection 1:*** 3.3V 14.318 MHz clock output. This pin also serves as the select strap to determine device's operating frequency as described in frequency Table. Pull high 120k.
REF_2	46	O	***Reference Clock2:*** 3.3V 14.318 MHz clock output.
X1	3	I	***Crystal Input:*** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	4	O	***Crystal Output:*** An input connection for an external 14.318MHz crystal connection. If using an external reference, this pin must be left unconnected.
PCIF/FS4*	9	O	***PCI Clock Free running /Frequency Selection 4 :*** 3.3V 33 MHz PCI clock outputs. Not affected by PCI_STOP#. This pin also serves as the select strap to determine device's operating frequency as described in frequency Table. Pull high 120k.
PCI-E	22	O	***Early PCI Clock:*** Lead 2 ns than general PCI bus clock
PCI0/SEL24_48#	10	I/O	***PCI Clock 0/SEL24_48#:*** 3.3V 33 MHz PCI clock output. This pin also serves as power-on latch for 24_48MHz frequency selection, "0" for 48MHz and "1" for 24MHz.
PCI 1:8	11, 13, 14, 16, 17, 18, 20, 21	O	***PCI Clock 1 through 8:*** 3.3V 33 MHz PCI clock outputs. PCI0:7.
SRESET#	24	OD	***SRESET#: R***eset output for watch dog & bounding option(open drain pad).
48MHz/FS2*	6	I/O	***48 MHz Clock Output/Frequency Selection 2***: 3.3V fixed 48 MHz, non-spread spectrum clock output. This pin also serves as the select strap to determine device's operating frequency as described in frequency Table. Pull high 120k.
24_48MHz/FS3*	7	I/O	***24 MHz Clock Output/Frequency Selection 3:*** 3.3V fixed 24 MHz, non-spread spectrum clock output. This pin also serves as the select strap to determine device's operating frequency as described in frequency Table. Pull high 120k.
PD# *	34	I	***Power Down Control:*** LVTTL compatible input that places the device in power down mode when held low. Pull high 120k.
PCI_STOP# *	35	I	***PCI stop Control: Stop all PCI clock except PCI-F*** when held low. Pull high 120k.
CPU_STOP# *	36	I	***CPU stop Control: Stop all CPU clock*** when held low. Pull high 120k.
AGP_STOP# *	44	I	***AGP stop Control: Stop all AGP clock*** when held low. Pull high 120k.
REF_STOP# *	45	I	***REF stop Control: Stop all REF clock*** when held low. Pull high 120k.
AGP0:2	26, 27, 28	O	***AGP Clock Outputs:*** 3.3V output clocks. The operating frequency is controlled by FS0:3.
CPUCLKC_CS CPUCLKT_CS	38, 39	O	***CPU Clock Outputs:*** Clock outputs for the host bus interface. Output frequencies depending on the configuration of FS0:3. Voltage swing is set by VDD2.5.**(PUSH/PULL)**
CPUCLKC0 CPUCLKT0	41, 42	OD	***CPU Clock Outputs:*** Clock outputs for the host bus interface. Output frequencies depending on the configuration of FS 0:4. Voltage swing is set by VDD2.5.**(OPEN_DRAIN)**
SDATA	31	I/O	Data pin for serial interface.
SCLK	30	I	Clock pin for serial interface.
VDD3.3	1, 5, 15, 23, 25, 33	P	***3.3V Power Connection:*** Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output buffers. Connect to 3.3V.
VDD2.5	40	P	***2.5V Power Connection:*** Power supply for IOAPIC and CPU output buffers. Connect to 2.5V or 3.3V.
GND	2, 8, 12, 19, 29, 32, 37, 43	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Note: Internal 120K pull-up[*] or pull down[**] resistors present. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.

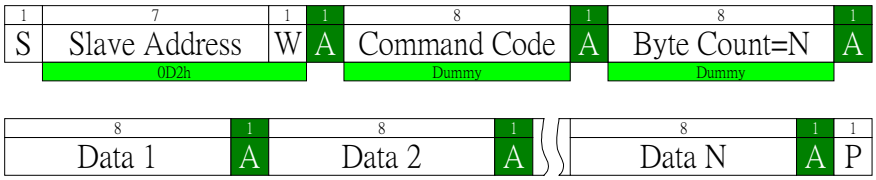
Frequency Selection:

s4	s3	s2	s1	s0	CPU	AGP	PCI
0	0	0	0	0	156.00	78.00	39.00
0	0	0	0	1	154.00	77.00	38.50
0	0	0	1	0	152.00	76.00	38.00
0	0	0	1	1	147.00	73.50	36.75
0	0	1	0	0	144.00	72.00	36.00
0	0	1	0	1	142.00	71.00	35.50
0	0	1	1	0	138.00	69.00	34.50
0	0	1	1	1	136.00	68.00	34.00
0	1	0	0	0	124.00	62.00	31.00
0	1	0	0	1	122.00	61.00	30.50
0	1	0	1	0	117.00	78.00	39.00
0	1	0	1	1	115.00	76.67	38.33
0	1	1	0	0	113.00	75.33	37.67
0	1	1	0	1	108.00	72.00	36.00
0	1	1	1	0	105.00	70.00	35.00
0	1	1	1	1	102.00	68.00	34.00
1	0	0	0	0	233.30	66.66	33.33
1	0	0	0	1	220.00	73.33	36.67
1	0	0	1	0	210.00	70.00	35.00
1	0	0	1	1	200.00	66.67	33.33
1	0	1	0	0	190.00	76.00	38.00
1	0	1	0	1	180.00	72.00	36.00
1	0	1	1	0	170.00	68.00	34.00
1	0	1	1	1	150.00	75.00	37.50
1	1	0	0	0	140.00	70.00	35.00
1	1	0	0	1	120.00	60.00	30.00
1	1	0	1	0	110.00	73.33	36.67
1	1	0	1	1	66.60	66.60	33.30
1	1	1	0	0	200.00	66.67	33.33
1	1	1	0	1	166.60	66.64	33.32
1	1	1	1	0	100.20	66.80	33.40
1	1	1	1	1	133.30	66.65	33.33

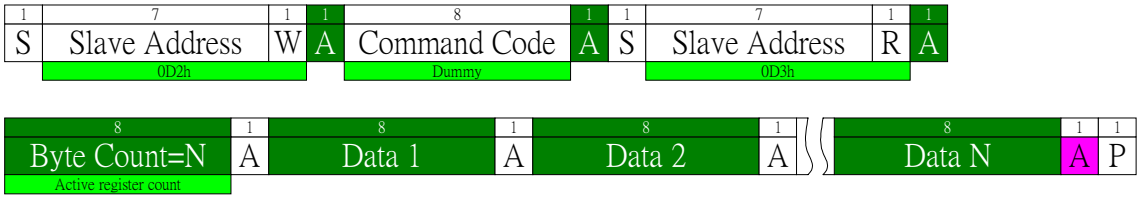
Standard Serial Bus Control:

Support standard serial bus block-mode and word-mode.

The Block Mode:

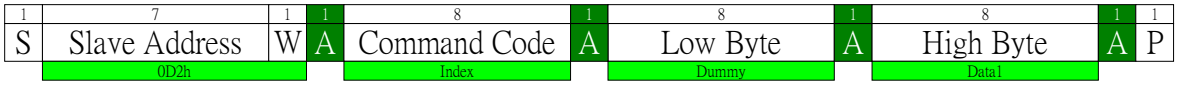


Block Write

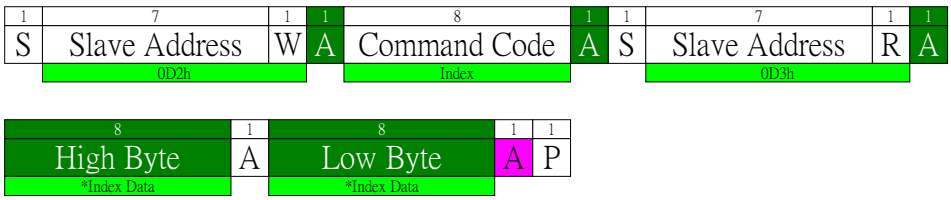


Block Read

The Word Mode:



Write Word



Read Word

Note slave address is D2h.

Register Description

CR 00h								
Bit	**Description**							**Default**
Bit7	0 = spread spectrum disable 1 = spread spectrum enable							0
BitX=0	**Bit2**	**Bit1**	**Bit6**	**bit5**	**bit4**	**CPU**	**AGP**	**PCI**	1
Bit2	0	0	0	0	0	157.00	78.50	39.25	
Bit1	0	0	0	0	1	155.00	77.50	38.75	0
Bit6	0	0	0	1	0	153.00	76.50	38.25	0
Bit5	0	0	0	1	1	148.00	74.00	37.00	0
Bit4	0	0	1	0	0	145.00	72.50	36.25	0
	0	0	1	0	1	143.00	71.50	35.75	
	0	0	1	1	0	139.00	69.50	34.75	0
	0	0	1	1	1	137.00	68.50	34.25	0
	0	1	0	0	0	125.00	62.50	31.25	0
	0	1	0	0	1	123.00	61.50	30.75	
	0	1	0	1	0	118.00	78.67	39.33	
	0	1	0	1	1	116.00	77.33	38.67	
	0	1	1	0	0	114.00	76.00	38.00	
	0	1	1	0	1	109.00	72.67	36.33	
	0	1	1	1	0	106.00	70.67	35.33	
	0	1	1	1	1	103.00	68.67	34.33	
	1	**0**	**0**	**0**	**0**	235.00	67.14	33.57	
	1	0	0	0	1	221.00	73.67	36.83	
	1	0	0	1	0	211.00	70.33	35.17	
	1	0	0	1	1	201.00	67.00	33.50	
	1	0	1	0	0	191.00	76.40	38.20	
	1	0	1	0	1	181.00	72.40	36.20	
	1	0	1	1	0	171.00	68.40	34.20	
	1	0	1	1	1	151.00	75.50	37.75	
	1	1	0	0	0	141.00	70.50	35.25	
	1	1	0	0	1	121.00	60.50	30.25	
	1	1	0	1	0	111.00	74.00	37.00	
	1	1	0	1	1	68.00	68.00	34.00	
	1	1	1	0	0	201.00	67.00	33.50	
	1	1	1	0	1	168.00	67.20	33.60	
	1	1	1	1	0	102.00	68.00	34.00	
	1	1	1	1	1	135.00	67.50	33.75	
bit3	0 = frequency is selected by latched input FS[4:0] 1 = frequency is selected by CR00h – bit 2, 1, 6, 5, 4								0
bit0	0 = running 1 = tristate all output								0

Note1: Default at power-up will be for latched logic inputs to define frequency, Bit 2,1,6:4 are default to 00000.

Note2: Bit X=CR10h bit3 default to 1.

CR 00h								
Bit	**Description**							**Default**
Bit7	0 = spread spectrum disable 1 = spread spectrum enable							0
Bitx=1	**Bit2**	**Bit1**	**Bit6**	**bit5**	**bit4**	**CPU**	**AGP**	**PCI**	1
Bit2	0	0	0	0	0	156.00	78.00	39.00	0
Bit1	0	0	0	0	1	154.00	77.00	38.50	0
Bit6	0	0	0	1	0	152.00	76.00	38.00	0
Bit5	0	0	0	1	1	147.00	73.50	36.75	0
Bit4	0	0	1	0	0	144.00	72.00	36.00	0
	0	0	1	0	1	142.00	71.00	35.50	0
	0	0	1	1	0	138.00	69.00	34.50	0
	0	0	1	1	1	136.00	68.00	34.00	0
	0	1	0	0	0	124.00	62.00	31.00	0
	0	1	0	0	1	122.00	61.00	30.50	
	0	1	0	1	0	117.00	78.00	39.00	
	0	1	0	1	1	115.00	76.67	38.33	
	0	1	1	0	0	113.00	75.33	37.67	
	0	1	1	0	1	108.00	72.00	36.00	
	0	1	1	1	0	105.00	70.00	35.00	
	0	1	1	1	1	102.00	68.00	34.00	
	1	**0**	**0**	**0**	**0**	233.30	66.66	33.33	
	1	0	0	0	1	220.00	73.33	36.67	
	1	0	0	1	0	210.00	70.00	35.00	
	1	0	0	1	1	200.00	66.67	33.33	
	1	0	1	0	0	190.00	76.00	38.00	
	1	0	1	0	1	180.00	72.00	36.00	
	1	0	1	1	0	170.00	68.00	34.00	
	1	0	1	1	1	150.00	75.00	37.50	
	1	1	0	0	0	140.00	70.00	35.00	
	1	1	0	0	1	120.00	60.00	30.00	
	1	1	0	1	0	110.00	73.33	36.67	
	1	1	0	1	1	66.60	66.60	33.30	
	1	1	1	0	0	200.00	66.67	33.33	
	1	1	1	0	1	166.60	66.64	33.32	
	1	1	1	1	0	100.20	66.80	33.40	
	1	1	1	1	1	133.30	66.65	33.33	
bit3	0 = frequency is selected by latched input FS[4:0] 1 = frequency is selected by CR00h – bit 2, 1, 6, 5, 4								0
bit0	0 = running 1 = tristate all output								0

Note1: Default at power-up will be for latched logic inputs to define frequency, Bit 2,1,6:4 are default to 00000.

Note2: Bit X=CR10h bit3 default to 1.

CR 01h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = CPUCLKT0/CPUCLKC0 stop 1 = CPUCLKT0/CPUCLKC0 running	42,41	R/W	1
Bit6	0 = CPUCLKT_CS, CPUCLKC_CS stop 1 = CPUCLKT_CS, CPUCLKC_CS running	39,38	R/W	1
Bit5	0 = 48MHz clock stop 1 = 48MHz clock running	6	R/W	1
Bit4	0 = 24_48MHz stop 1 = 24_48MHz running	7	R/W	1
Bit3	Reserved			1
Bit2	0 = AGPCLK2 stop 1 = AGPCLK2 running	28	R/W	1
Bit1	0 = AGPCLK1 stop 1 = AGPCLK1 running	27	R/W	1
Bit0	0 = AGPCLK0 stop 1 = AGPCLK0 running	26	R/W	1

CR 02h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = PCICLK7 clock stop 1 = PCICLK7 clock running	20	R/W	1
Bit6	0 = PCICLK6 clock stop 1 = PCICLK6 clock running	18	R/W	1
Bit5	0 = PCICLK5 clock stop 1 = PCICLK5 clock running	17	R/W	1
Bit4	0 = PCICLK4 clock stop 1 = PCICLK4 clock running	16	R/W	1
Bit3	0 = PCICLK3 clock stop 1 = PCICLK3 clock running	14	R/W	1
Bit2	0 = PCICLK2 clock stop 1 = PCICLK2 clock running	13	R/W	1
Bit1	0 = PCICLK1 clock stop 1 = PCICLK1 clock running	11	R/W	1
Bit0	0 = PCICLK0 clock stop 1 = PCICLK0 clock running	10	R/W	1

CR 03h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = PCICLK_F clock stop 1 = PCICLK_F clock running	9	R/W	1
Bit6	0 = PCICLK_E clock stop 1 = PCICLK_E clock running	22	R/W	1
Bit5	Reserved			1
Bit4	0 = PCICLK8 clock stop 1 = PCICLK8 clock running	21	R/W	1
Bit3	0 = REF_F clock stop 1 = REF_F clock running	46	R/W	1
Bit2	Reserved			1
Bit1	0 = REF_1 clock stop 1 = REF_1 clock running	47	R/W	1
Bit0	0 = REF_0 clock stop 1 = REF_0 clock running	48	R/W	1

CR 04h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved		R/W	1
Bit6	Reserved		R/W	1
Bit5	Reserved		R/W	1
Bit4	Reserved		R/W	1
Bit3	Reserved		R/W	1
Bit2	Reserved		R/W	1
Bit1	Reserved		R/W	1
Bit0	Reserved		R/W	1

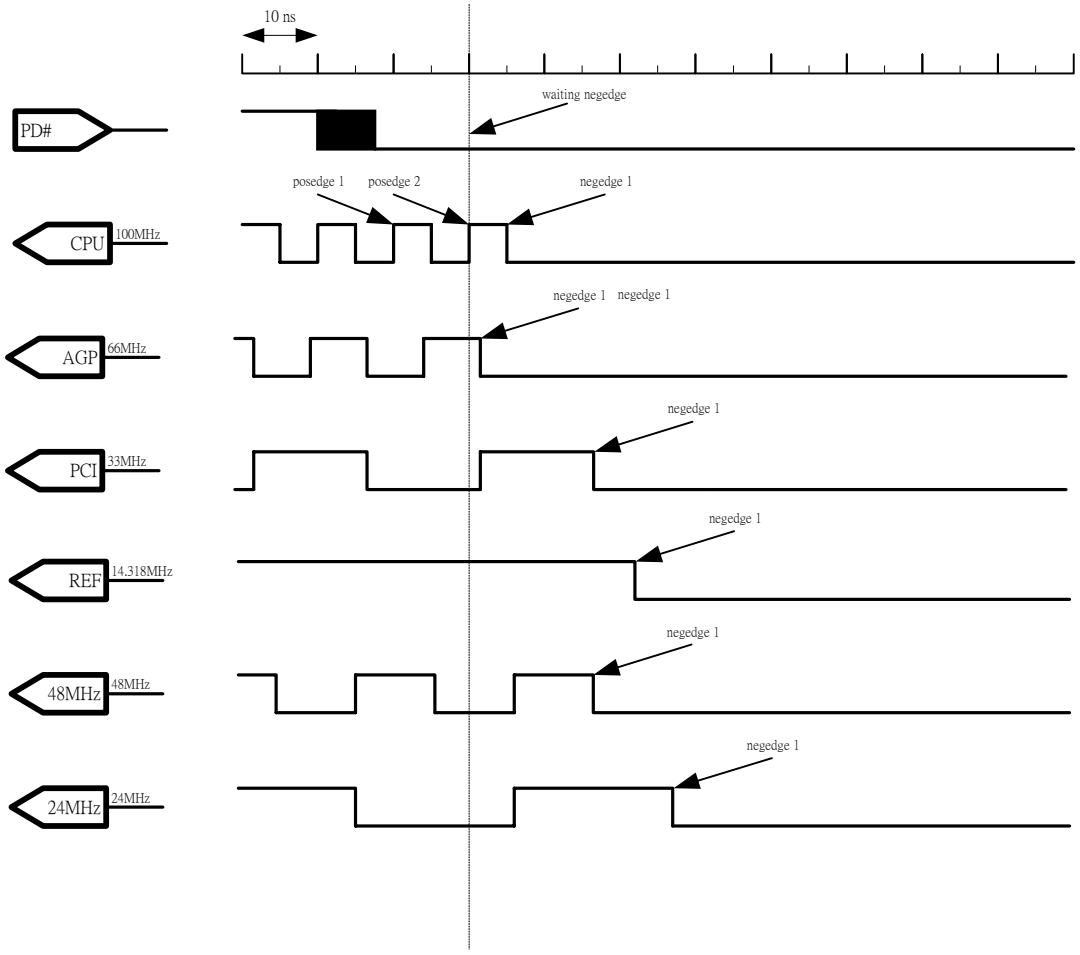
CR 05h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Power on FS4 latched	9	R	Latched
Bit6	Power on FS3 latched	7	R	Latched
Bit5	Power on FS2 latched	6	R	Latched
Bit4	Power on FS1 latched	47	R	Latched
Bit3	Power on FS0 latched	48	R	Latched
Bit2	Reserved		R/W	1
Bit1	Reserved		R/W	1
Bit0	Reserved		R/W	1

CR 06h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved	R/W		1
Bit6	Reserved	R/W		1
Bit5	Reserved	R/W		1
Bit4	Reserved	R/W		1
Bit3	Reserved	R/W		1
Bit2	Reserved	R/W		1
Bit1	Reserved	R/W		1
Bit0	Reserved	R/W		1

Power Down Function

PD#	CPUCLK	AGP	PCICLK	REF	24MHz	48MHz	Osc	VCOs
0	Low	Low	Low	Low	Low	Low	Off	Off
1	On	On	On	On	On	On	On	On

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLK, all the output clocks are driven Low on their next High to Low transition.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	13.5	20	45	Ω
Output High Voltage		IOH = -1 mA	2			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 2.375V	-27		-27	mA
Output Low Current		VOL @MIN= 1.2V , VOL@ MAX= 0.3V	27		30	mA
Rise Time		VOL = 0.4 V, VOH = 2.0 V	0.4		1.6	ns
Fall Time		VOH = 2.0 V, VOL = 0.4 V	0.4		1.6	ns
Duty Cycle		VT = 1.25 V	45	50	55	%
Skew		VT = 1.25 V			250	ps
Jitter		VT = 1.25 V			250	ps

Electrical Characteristics - AGP

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	12	20	55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.55	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-33		-33	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	30		38	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.4		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.4		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics - PCI

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	12	20	55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-33		-33	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	30		38	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics - IOAPIC

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	12	20	30	Ω
Output High Voltage		IOH = -5 mA	2			V
Output Low Voltage		IOL = 9 mA			0.4	V
Output High Current		VOH @MIN= 1.4V , VOH@ MAX= 2.375V	-36		-21	mA
Output Low Current		VOL @MIN= 1.0V , VOL@ MAX= 0.2V	31		36	mA
Rise Time		VOL = 0.4 V, VOH = 2.0 V	0.4		2	ns
Fall Time		VOH = 2.0 V, VOL = 0.4 V	0.4		2	ns
Duty Cycle		VT = 1.25 V	45	50	55	%
Jitter		VT = 1.25 V			500	ps

Electrical Characteristics - REF

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				14.318		MHz
Output Impedance		VO = VDD*(0.5)	10	20	45	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 2.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 1.0V , VOL@ MAX= 0.4V	27		30	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	1	1.8	4	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	1	1.8	4	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Jitter		VT = 1.5 V			1000	ps

Electrical Characteristics - 48MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

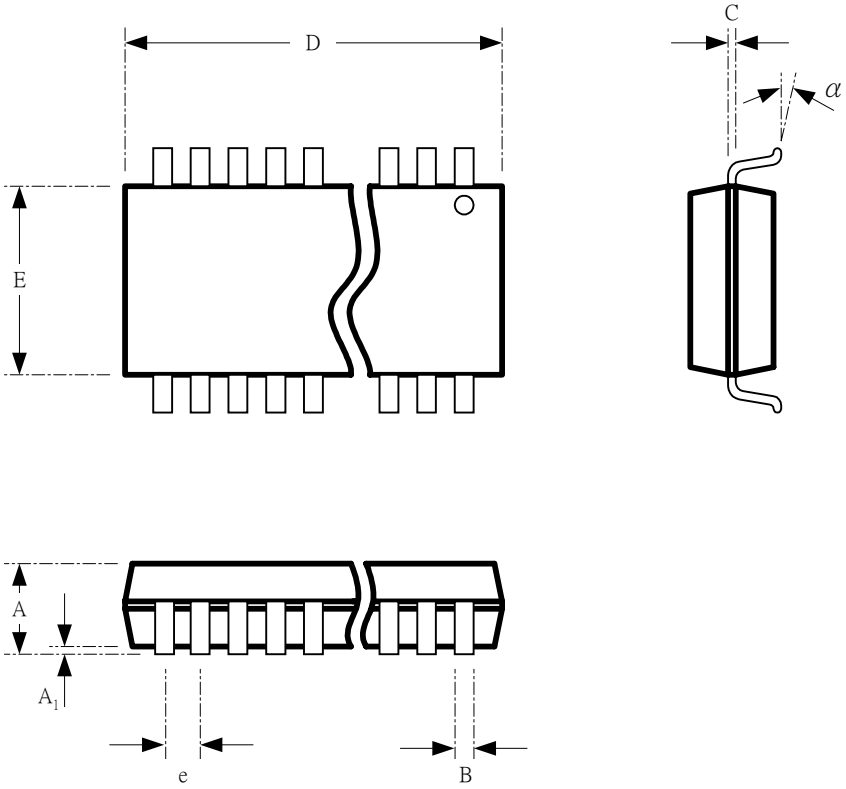
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				48		MHz
Output Impedance		VO = VDD*(0.5)	10	20	45	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 2.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 1.0V , VOL@ MAX= 0.4V	27		30	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	1	1.8	4	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	1	1.8	4	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics - 24MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				24		MHz
Output Impedance		VO = VDD*(0.5)	10	20	45	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 2.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 1.0V , VOL@ MAX= 0.4V	27		30	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	1	1.8	4	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	1	1.8	4	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Jitter		VT = 1.5 V			500	ps

Package outline



SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Min.	Type	Max.		Min.	Type	Max.	
A	0.095	0.101	0.110	AC	0.620	0.625	0.630	48
A1	0.008	0.012	0.016	AD	0.720	0.725	0.730	56
B	0.008	0.010	0.0135					
C	0.005	0.0075	0.010					
D	See Variations							
E	0.292	0.296	0.299					
e	0.025BSC							
α	0°	5°	10°					

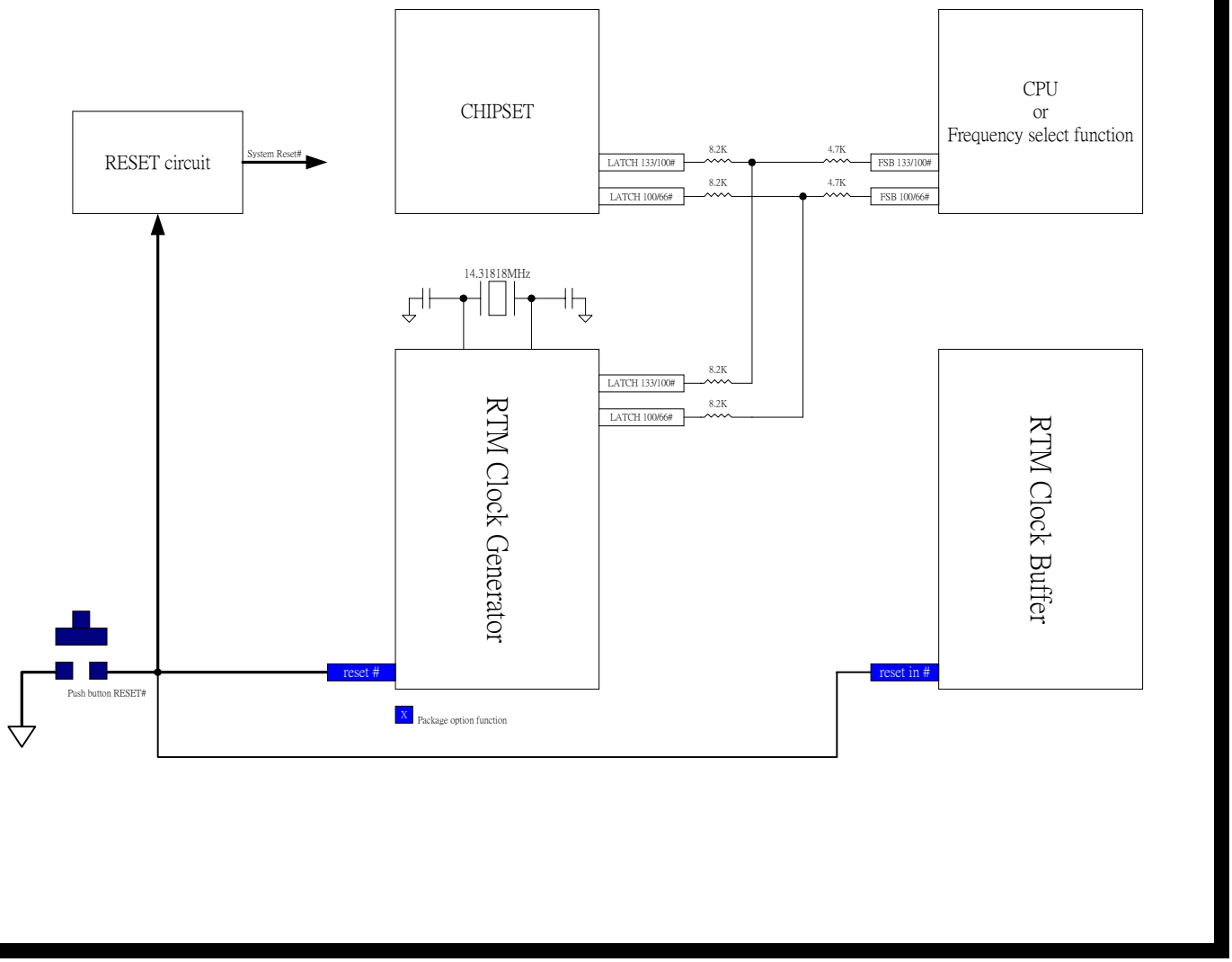
General Description enhance partial

The RTM 560-266R family enhance function will be build for VIA KT 266 system.

Features

- Support Up to 400 MHz output frequency.
- Power Down feature.
- Down Spread Spectrum for EMI control.
- 2 PLL circuit with 1 programmable PLL
- 9 PCI 2X driving strength
- Watch dog for reset output (by bounding option)
- Programmable watch dog timer
- Fs0..Fs3 internal pull High/Low 120k PMOS/NMOS resistor
- Fs0..Fs3 latched data could be read back
- Programmable Clock skew
- Programmable PCI divider
- Programmable PLL coefficient
- Reserved register for compatible
- Programmable Down/Center spread spectrum
- Reset # open drain pad output pin
- CPU SDRAM PCI global stop
- Power down function by enhance register also
- Driving strength MASK option
- Low jitter VCO technology with ring oscillator 1GHz
- Internal clock divider for test mode

Demo board circuit:



Quartz crystal requirements for RTM560 series.

1. Frequency and Oscillation Circuits

RTM560 series are designed to work from a crystal with 14.31818MHz.
Fig-1 shows the equivalent circuits of crystal and oscillation circuits within RTM560 series.

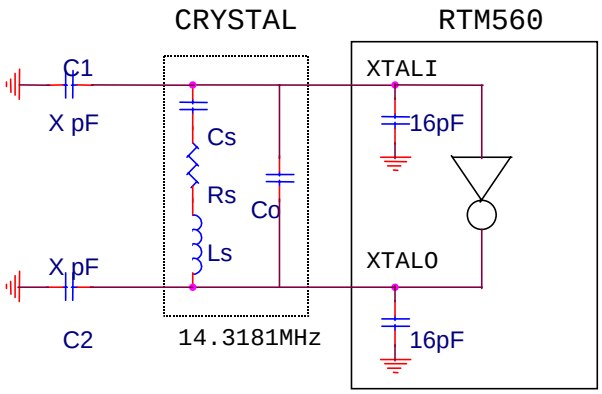


Fig-1 oscillation circuits

$$Fs \cong \frac{1}{2\pi\sqrt{Ls * Cs}}$$

The series resonant frequency, and parallel resonant frequency

$$Fp \cong \frac{1}{2\pi\sqrt{\frac{Ls * Cs * Co}{Cs + Co}}}$$

The oscillated frequency between *Fs* and *Fp*

$$Fo = Fs * \sqrt{1 + \frac{Cs}{Co + CL}}$$

where CL=((C1+16pF)*(C2+16pF)) / ((C1+16pF)+(C2+16pF))

2. Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	14.31818 MHz
Oscillation Mode	Fundamental
Load Cap. (CL)	16 ~32 pF
Freq. Tolerance(25℃)	+/- 30 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 Mohm min. at DC 100V

Table-1 Crystal General Specification

3. Load Capacitance (CL)

To operate between Fs and Fp requires external load capacitance. Although RTM560 series has embed internal 16 pF capacitors at XTALI and XTALO, the oscillated frequency may be a little higher than 14.31818 MHz if no C1 and C2 placed.

To reduce the REF clock jitter and get more accurate frequency, the external capacitor C1 and C2 must be used.

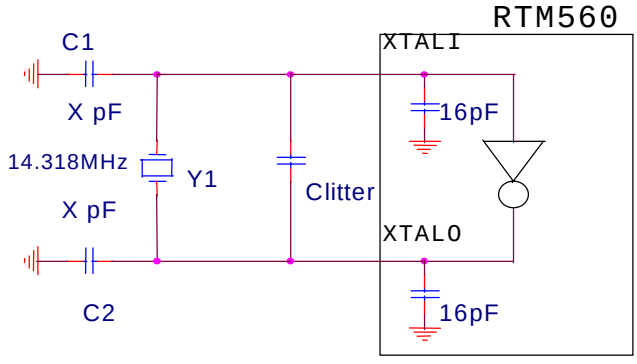


Fig-2 Clitter due to PCB Trace

In ideal case, ignore the Clitter at suggested C1=C2=16pF, the equivalent load capacitance is

$$CL = ((16\,pF + 16\,pF) * (16\,pF + 16\,pF)) / ((16\,pF + 16\,pF) + (16\,pF + 16\,pF)) = 16\,pF$$

According to Table-1 specification, the crystal with *CL* is 16pF is adapted. But in most case, the litter capacitor (Clitter) generated by PCB trace is existent. So the real CL is

$$CL = (C1 + 16\,pF) // (C2 + 16\,pF) + Clitter$$

Consider the litter capacitance , crystal with CL=20pF is allowable.

4. Reference table

C_L (pF)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
C_1=C_2 (pF)	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48

Table-2 Crystal C_L General Specification

Enhance register

CR 07h [7]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	1
Bit6	Reserved	R/W	1
Bit5	Reserved	R/W	1
Bit4	Reserved	R/W	1
Bit3	Reserved	R/W	1
Bit2	Reserved	R/W	1
Bit1	Reserved	R/W	1
Bit0	Reserved	R/W	1

CR 08h [8]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	1
Bit6	Reserved	R/W	1
Bit5	Reserved	R/W	1
Bit4	Reserved	R/W	1
Bit3	Reserved	R/W	1
Bit2	Reserved	R/W	1
Bit1	Reserved	R/W	1
Bit0	Reserved	R/W	1

CR 10h [16]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Version ID	R	0
Bit6	Version ID	R	0
Bit5	Version ID	R	0
Bit4	Version ID	R	0
Bit3	MSB of internal frequency selection table == bitX 1 = select ROM 20h..3fh 0 = select ROM 00h..1fh	R/W	Latched 1
Bit2	0 = normal 1 = watch dog enable. Action is internal reset & external reset 300 ms	R/W	0
Bit1	0 = serial Bus block mode 1 = serial Bus word mode	R/W	0
Bit0	0 = write protected CR[11h:24h] 1 = writable CR[11h:24h]	R/W	0

CR 11h [17]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	M code bit[7:0] for PLL1	R/W	[0110_0100]

CR 12h [18]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	M code bottom level bit[7:0] for PLL1 sperad spectrum	R/W	[0110_0100]

CR 13h [19]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	N code bit[7:0] for PLL1	R/W	[0001_0111]

** CPU Frequency = 24*(M+1)/(N+1) … N>1 (CPU/AGP = 66/66, 100/66, 133/66, 166/66)*

** CPU Frequency = 48*(M+1)/(N+1) … N>1 (CPU/AGP = 200/66, 233/66, 266/66)*

CR 14h [20]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[0000_0000]

CR 15h [21]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[0000_0000]

CR 16h [22]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[0000_0000]

CR 17h [23]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:4]	Reserved	R/W	[1111]
Bit3	1 = Output Disable for FSB_133/100# (FS4) & FSB_100/66# (FS3) 0 = Output Enable for FSB_133/100# (FS4) & FSB_100/66# (FS3)	R/W	1
Bit2	0 = normal 1 = enable auto reset CR10h-bit[1:0] & CR17h-bit[2] while CR17h-bit[0] being writen 1	R/W	0
Bit1	0 = disable last serial BUS write latched with reset# output 1 = enable last serial BUS write latched with reset# output & reset CR10h	R/W	0
Bit0	M N code latching buffer while writen 1	W	0

CR 18h [24]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit6	Reserved	R/W	0
Bit[5:0]	Reserved	R/W	[000000]

CR 19h [25]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:5]	Watch dog tmer [base =1.17 second] [000] = 3 base second [001] = 4 base second [010] = 5 base second [011] = 6 base second [100] = 7 base second [101] = 8 base second [110] = 9 base second [111] = 10base second	R/W	[001]
Bit4	0 = power down 1 = power on	R/W	1
Bit[3:0]	Reserved	R/W	[0000]

CR 1ah [26]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Cp_1 Base = 5 pF 0 = disconnect 1 = parallel Cp_1 with 5 pF	R/W	1
Bit6	0 = disconnect 1 = parallel Cp_1 with 5 pF	R/W	1
Bit5	0 = disconnect 1 = parallel Cp_1 with 5 pF	R/W	1
Bit4	0 = disconnect 1 = parallel Cp_1 with 5 pF	R/W	1
Bit3	I_1 Base = 0.5uA 0 = disconnect 1 = parallel I_1 with 4 uA	R/W	0
Bit2	0 = disconnect 1 = parallel I_1 with 2 uA	R/W	0
Bit1	0 = disconnect 1 = parallel I_1 with 1 uA	R/W	0
Bit0	0 = disconnect 1 = parallel I_1 with 0.5 uA	R/W	0

CR 1bh [27]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit6	0 = disconnect 1 = R_1 = 2000//2000	R/W	1
Bit5	0 = disconnect 1 = R_1 = 2000//1000	R/W	0
Bit4	0 = disconnect 1 = R_1 = 2000//500	R/W	0
Bit3	Cs_1 Base = 250 pF 0 = disconnect 1 = parallel Cs_1 with 50 pF	R/W	1
Bit2	0 = disconnect 1 = parallel Cs_1 with 50 pF	R/W	1
Bit1	0 = disconnect 1 = parallel Cs_1 with 50 pF	R/W	1
Bit0	0 = disconnect 1 = parallel Cs_1 with 50 pF	R/W	1

CR 1ch [28]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[0000-0000]

CR 1dh [29]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[0000-0000]

CR 1eh [30]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Cp_2 Base = 5 pF 0 = disconnect 1 = parallel Cp_2 with 5 pF	R/W	1
Bit6	0 = disconnect 1 = parallel Cp_2 with 5 pF	R/W	1
Bit5	0 = disconnect 1 = parallel Cp_2 with 5 pF	R/W	1
Bit4	0 = disconnect 1 = parallel Cp_2 with 5 pF	R/W	1
Bit3	I_2 Base = 0.3uA 0 = disconnect 1 = parallel I_2 with 96A	R/W	0
Bit2	0 = disconnect 1 = parallel I_2 with 48uA	R/W	0
Bit1	0 = disconnect 1 = parallel I_2 with 24uA	R/W	1
Bit0	0 = disconnect 1 = parallel I_2 with 12uA	R/W	1

CR 1fh [31]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:5]	000 = AGP select /2 (CPU = 66) 001 = AGP select /3 (CPU = 100) 010 = AGP select /4 (CPU = 133) 011 = AGP select /5 (CPU = 166, 110) 100 = AGP select /6 (CPU = 200) 101 = AGP select /7 (CPU = 233) 110 = AGP select /8 (CPU = 266) not support 111 = reserved	R/W	ROM/REG [010]
Bit[4:3]	00 = CPU select /2 (CPU= 66, 100, 133, 166) 01 = CPU select /1 (CPU=200, 233, 266) 10 = CPU select /3 (CPU=110) 11 = X	R/W	ROM/REG [00]
Bit2	0 = CPU/AGP divider select by ROM 1 = CPU/AGP divider select by CR1fh bit [7:3]	R/W	0
Bit1	1=PLL1 OP switch off 0=PLL1 OP switch on	R/W	1
Bit0	0=PLL1 programmable disable 1=PLL1 programmable enable	R/W	0

CR 20h [32]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit[6:4]	R_2 = 600Ωx ([6:4]+1)	R/W	[000]
Bit3	Cs_2 Base = 25pF 0 = disconnect 1 = parallel Cs_2 with 25pF	R/W	1
Bit2	0 = disconnect 1 = parallel Cs_2 with 25pF	R/W	1
Bit1	0 = disconnect 1 = parallel Cs_2 with 25pF	R/W	1
Bit0	0 = disconnect 1 = parallel Cs_2 with 25pF	R/W	1

CR 21h [33]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit6	0 = PCI to AGP delay 2.0ns except PCI-Early 1 = PCI to AGP delay 4.0ns except PCI-Early	R/W	0
Bit[5:4]	CPU group delay selection by 150 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[3:2]	Reserved delay selection by 150 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[1:0]	AGP group delay selection by 150 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]

CR 22h [34]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	PCI group delay selection by 150 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[5:4]	PCI-F delay selection by 150 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit3	0 = normal 1 = enable test mode (PLL1) = (PLL1)/4 & Watch Dog timer base =1u second	R/W	0
Bit[2:0]	Spread spectrum change level by (ref / N) base [000] 8 base clock [001] 16 base clock [010] 32 base clock [011] 64 base clock [100] 128 base clock [101] 256 base clock [110] 512 base clock [111] 1024 base clock	R/W	[010]

CR 23h [35]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[1111-1111]

CR 24h [36]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved	R/W	[1111-1111]